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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,790	01/21/2004	Albert E. Cosand	PD-03W012	3552

7590 08/02/2006

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/761,790	**Applicant(s)** COSAND, ALBERT E.	
	Examiner Khai M. Nguyen	**Art Unit** 2819	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 7/21/2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 56-83.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☒ Other: see paper attached herewith.

Khai M. Nguyen
Art Unit: 2819
571-272-1809

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 56-58, 60-81, and 82 are rejected under 35 U.S.C. 102(b) as being anticipated by Cake et al. (US 6,292,121).

Regarding claim 56, Cake et al. discloses (Figs. 5-6, 10-13) a delta-sigma modulator (see, the title) comprising:

a loop filter (resonator 315 of Fig. 11 or integrator 320 of Fig. 13) (Cake uses the term "resonator 25 in place of the integrator" which acts or functions as a loop filter (12) of the claim invention – see, col. 9, lines 49-60; and col. 6, lines 44-67);

a comparator (comparator 43 of a comparator/latch circuit as shown in Fig. 10 and/or comparator 630 or 640 of Fig. 6) coupled to the loop filter (i.e., the resonator or integrator as shown in various Figures);

and a switch (including transistor pairs 652/654, 653/655, and 656/658 of Fig. 6 – col. 6, lines 15-20) electrically coupled to the comparator and the loop filter (Fig. 6), wherein the switch comprising:

first means (i.e., the latch portion, see Fig. 10, of comparator/circuit 630 of Fig. 6) for providing a first set of first and second complementary intermediate signals (differential output signals of the comparator/latch 630 of Fig. 6);

second means (the latch portion, see Fig. 10, of comparator/latch circuit 640 of Fig. 6) for providing a second set of third and fourth complementary intermediate signals (differential output signals of the comparator/latch 640 of Fig. 6);

third means (differential transistor pair 652/654 of Fig. 6) responsive to the first set of signals (received at their gates or bases) for providing complementary output signals (at collector nodes of transistor pair 652/654);

fourth means (differential transistor pair 656/658) responsive to the second set of signals (received at their gates or bases) for providing complementary output signals (at collector nodes of 656/658); and

fifth means (differential transistor pair 653/655) for selectively activating (col. 6, lines 41-43) the third means (differential transistor pair 652/654 of Fig. 6) or the fourth means (differential transistor pair 656/658) in response to a control signal (a sampling clock signal from a source 620) to switch signals (current signals at collectors of transistors 613/614) from the loop filter in response, at least in part, to signals (Dout1 and/or Dout2) from the comparator (630 and/or 640) (Fig. 6; line 60 of col. 6 to line 33 of col. 7).

Regarding claims 57-58, Cake et al. discloses wherein the recited first means (of claim 56) corresponds to a master latch (i.e., the latch portion of first comparator/latch circuit 630 of Fig. 6); and the recited second means corresponds to a slave latch (i.e., the latch portion of second comparator/latch circuit 640 of Fig. 6).

Regarding claims 60-65, Cake et al. discloses the third means (of claim 56) including first and second transistors (the field effect transistors 652/654), which are connected in a common emitter configuration, (see Fig. 6), wherein the field effect transistors 652/654 are for formed by N-type and P-type semiconductor materials.

Regarding claim 66, Cake et al. discloses the invention of claim 61 wherein a first intermediate signal (first output of the first means) is provided as an input to the first transistor (transistor 652 of Fig. 6) and a second intermediate signal (second output of the first means) is provided as an input to the second transistor (654 of Fig. 6).

Regarding claims 67-72, Cake et al. discloses the fourth means (of claim 61) including third and fourth transistors (the field effect transistors 656/658), which are connected in a common emitter configuration, (see Fig. 6), wherein the field effect transistors 656/658 are for formed by N-type and P-type semiconductor materials.

Regarding claim 73, Cake et al. discloses the invention of claim 68 wherein a third intermediate signal (first output of the second means) is provided as an input to the third transistor (transistor 656 of Fig. 6) and a fourth intermediate signal (second output of the second means) is provided as an input to the fourth transistor (658 of Fig. 6).

Regarding claims 74-79, Cake et al. discloses the invention of claim 67 wherein the fifth means (differential field effect transistor pair 653/655) includes a fifth transistor

(653) and a sixth transistor (655) which are connected in a common emitter configuration (Fig. 6), wherein the field effect transistors 653/655 are for formed by N-type and P-type semiconductor materials.

Regarding claim 80, Cake et al. discloses the invention of claim 75 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals (column 7, lines 24-33).

Regarding claims 81-82, Cake et al. discloses the invention of claim 80 wherein the fifth (first) and sixth transistors (653/655) have a terminal connected to a current source (650) and a terminal connected to one of the first differential pair (652/654) and the second differential pair (656/658).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cake et al. (US 6,292,121) in view of Cheng (US 6,396,428). Cake et al. discloses the delta-sigma modulator of the claimed invention (of claims 56-58) except for the first and second latches are coupled in series as claimed. Cheng discloses (Fig. 1) a delta-sigma modulator (see the title & abstract) comprising a resonator 10 (column 3, lines 4-12), a

clocked comparator (11A), a first or master latch (11B), and a second or slave latch (11C) serially connected to the first latch (column 3, lines 39-41). Thus, it would have been obvious to one person having ordinary skills in the art at the time the invention was made to modify the connection of the latches (of circuits 330/630 and 340/640) as suggested by Cheng (see Fig. 1) for improving the noise shaping of the delta-sigma modulator (column 3, lines 20-25).

Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cake et al. (US 6,292,121) in view of Watson (US 6,445,322). Cake et al. discloses the claimed invention (82) except for the current source is a cascode current source. Watson discloses an apparatus (see Fig. 1B or 2) wherein a DAC current switch or steering cell (transistor pair 102a/b or 204/205 which is equivalent to the means) is coupled to a cascode current source (103/151 or 210). Therefore, it would have been obvious to one person having ordinary skills in the art at the time the invention was made to use a cascode current source as suggested by Watson for providing a current to the fifth means (of claim 56) because the cascode current source has high output impedance, therefore, a high noise immunity is achieved with respect to noise in the output terminal of the current source (column 1, lines 33-41).

Response to Arguments/Remarks

3. Applicant's arguments or remarks filed May 17th 2006 have been fully considered but they are not persuasive. The applicant argues (see pages 6-7 of the remarks) the applied reference does not disclose an arrangement in which the switch is coupled to

the loop filter so that the switch is effective to switch signals from the loop filter in response signals from the comparator. As best understood by the examiner, the [loop] filter as disclosed by the applicant is an active filter with transconductors and integrators (paragraph [0020] and Fig. 1). As already pointed out (see above), Cake fully discloses the claimed invention wherein the integrator as shown in Figs. 1-3, 5, 10, and 13 can be replaced by a resonator, which functions as a filter (col. 9, lines 40-60; and Figs. 11-12). Cake also discloses transistors 613-616, resistor 617, current sources 610, 611, 618, 619, and capacitor 612 of Fig. 6 form a transconductance circuit (col. 6, lines 44-67), which is equivalent to the loop filter 12 as defined by the applicant's disclosure. For these reasons, the rejection of pending claims is maintained.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

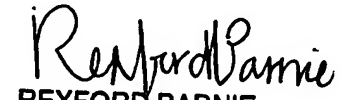
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford (Rex) Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khai M. Nguyen
Art Unit: 2819

571-272-1809



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